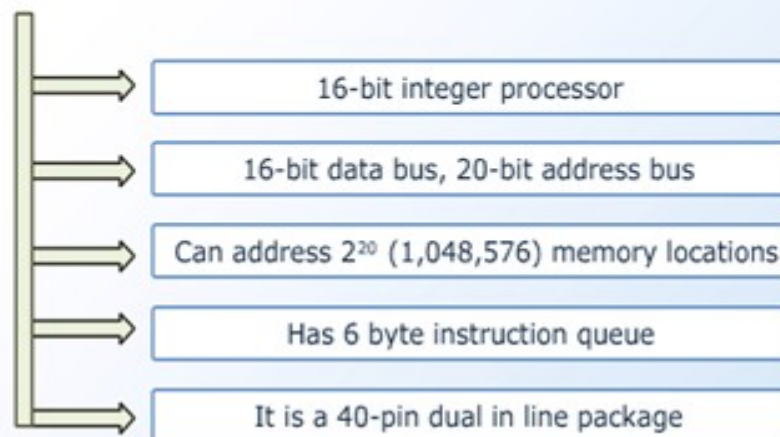# MPMC SUMMARY

Microprocessor Evolution

- Microprocessor was invented in 1971 by Intel
- It evolved from the inventions of Transistor and Integrated Circuits
- The ever increasing requirement of better and faster performance has led to evolve more microprocessors with more capabilities than the earlier one
- Microprocessor finds its application from fastest computers to simplest toys
- Today the microprocessor represents the most complex application of transistor, with some most powerful microprocessors having more than 10 million transistors

8086 – Important Points

Avfter having a brief overview of 8085, let us now refresh few points about 8086 microprocessor

- 16-bit integer processor
- 16-bit data bus, 20-bit address bus
- Can address 2^{20} (1,048,576) memory locations
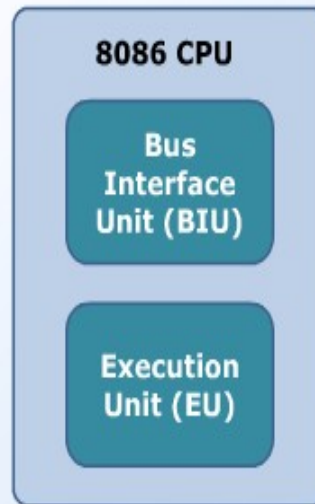- Has 6 byte instruction queue
- It is a 40-pin dual in line package
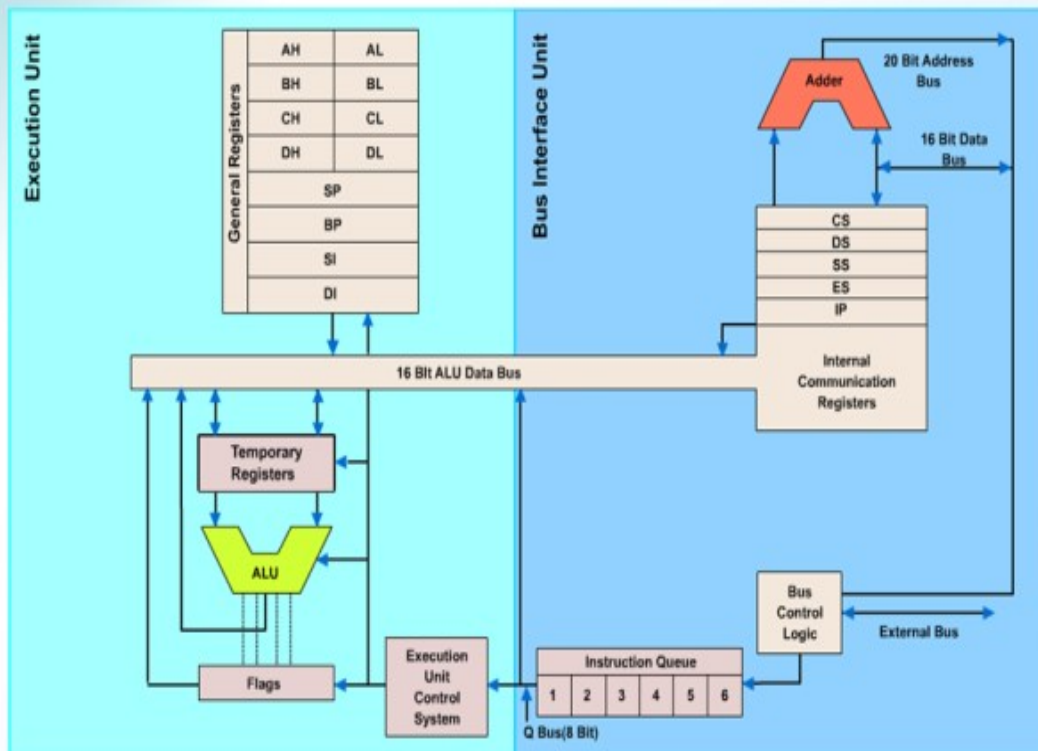
8086 – Important Points

Before learning programming and other details of 8086 let us first understand its internal architecture.

8086 is divided into two parts as

1. **Bus Interface Unit**

2. **Execution Unit**

8086 CPU

Bus Interface Unit (BIU)

Execution Unit (EU)
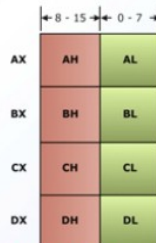
8086 – Internal Architecture

Register Organization

➤ The 8086 contains fourteen 16-bit registers. They are classified as:

- General Purpose Registers
- Segment Registers
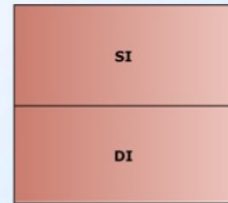- Index Registers
- Pointer Registers
- Flag Registers

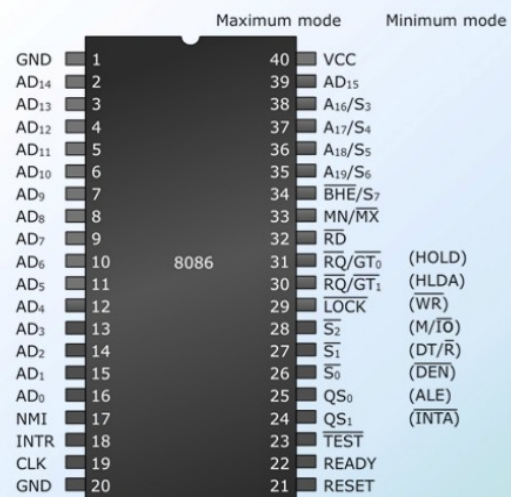**General Data Registers**

Segment Registers

Index Registers

Pointer Registers

Status flags

Control flags

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	O	D	I	T	S	Z	X	Ac	X	P	X	Cy

Flag Registers

Click to view animation

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Signal Description of 8086

➤ The 8086 has two operating modes: Minimum mode and Maximum mode

➤ If MN/$\overline{MX}$ pin is high it is said to be operated in Minimum mode

➤ If MN/$\overline{MX}$ pin is low it is said to be operated in Minimum mode

Maximum mode   Minimum mode

GND	1	40 VCC
AD14	2	39 AD15
AD13	3	38 A16/S3
AD12	4	37 A17/S4
AD11	5	36 A18/S5
AD10	6	35 A19/S6
AD9	7	34 $\overline{BHE}$/S7
AD8	8	33 MN/$\overline{MX}$
AD7	9	32 $\overline{RD}$
AD6	10	31 $\overline{RQ}$/$\overline{GT_0}$ (HOLD)
AD5	11	30 $\overline{RQ}$/$\overline{GT_1}$ (HLDA)
AD4	12	29 $\overline{LOCK}$ ($\overline{WR}$)
AD3	13	28 $\overline{S_2}$ (M/$\overline{IO}$)
AD2	14	27 $\overline{S_1}$ (DT/$\overline{R}$)
AD1	15	26 $\overline{S_0}$ ($\overline{DEN}$)
AD0	16	25 QS0 (ALE)
NMI	17	24 QS1 ($\overline{INTA}$)
INTR	18	23 $\overline{TEST}$
CLK	19	22 READY
GND	20	21 RESET

8086

Pin Diagram of 8086

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8255 PIO/PPI

PIO- PARALLEL INPUT OUTPUT PORT**;**   **PPI-** PROGRMABLE PERIPH

It is designed for use with Intel's 8-bit, 16-bit and higher capacity
It has 24 I/O lines - two groups (Group-A & Group-B) each of 12 I/O
Group-A:- contains an - 8-bit PORT- A (PA0 – PA7)
                                      - 4-bit upper PORT-C (PC4 – PC7)
Group-B:- contains an - 8-bit PORT- B (PB0 – PB7)
                                      - 4-bit lower PORT-C (PC0 – PC3)
All these ports can function independently either as **input or a**
(PA0 – PA7): these lines acts as either latched output or buffered
(PC4 – PC7): these lines acts as either latched output or buffered
(PC0 – PC3): these lines acts as either latched output or buffered
(PB0 – PB7): these lines acts as either latched output or buffered

input lines (CWR)
RD ' : input (by 8086)- low to indicate read operation to 8255
WR ' : input (by 8086)- low to indicate write operation
CS ' : chip select
D0 -D7: these are data lines those carry data or control word to/fr
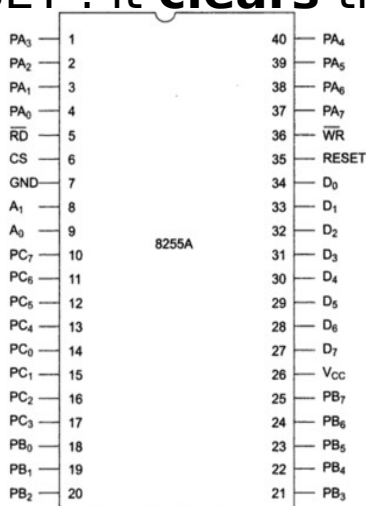RESET : it **clears** the **control word register** of 8255 , all ports a
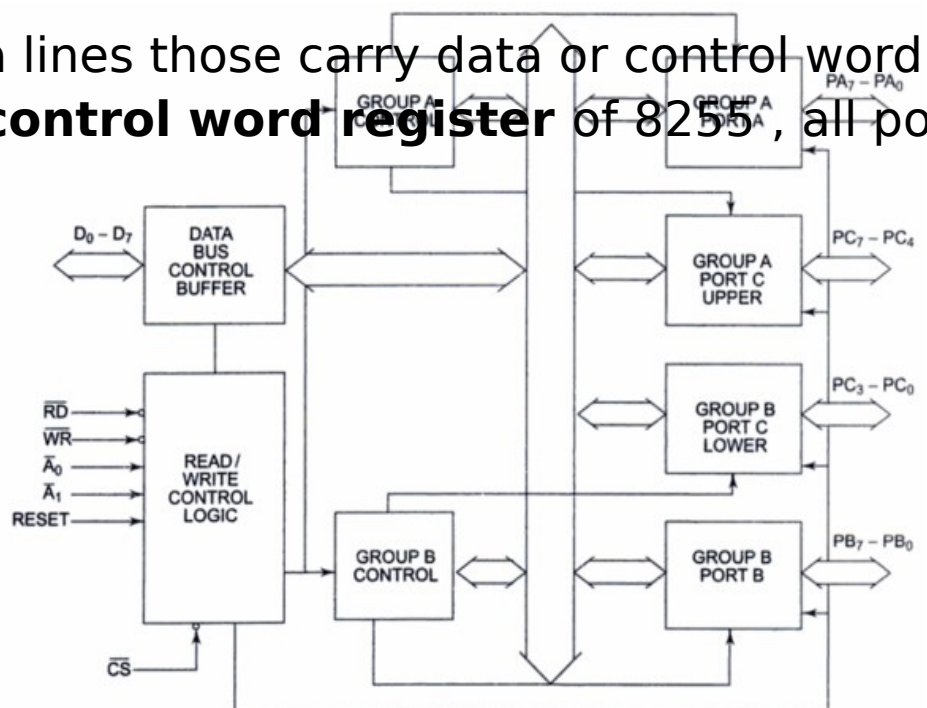

Fig. 5.17(b) 8255A Pin Configuration

Fig. 5.17(a)   8255 Internal Architecture

No.	Microprocessor	Microcontroller
1.	Microprocessor contains ALU, control unit (clock and timing circuit), different register and interrupt circuit.	Microcontroller contains microprocessor, memory (ROM and RAM), I/O interfacing circuit and peripheral devices such as A/D converter, serial I/O, timer etc.
2.	It has many instructions to move data between memory and CPU.	It has one or two instructions to move data between memory and CPU.
3.	It has one or two bit handling instructions.	It has many bit handling instructions.
4.	Access times for memory and I/O devices are more.	Less access times for built-in memory and I/O devices.
5.	Microprocessor based system requires more hardware.	Microcontroller based system requires less hardware reducing PCB size and increasing the reliability.
6.	Microprocessor based system is more flexible in design point of view.	Less flexible in design point of view.
7.	It has single memory map for data and code.	It has separate memory map for data and code.
8.	Less number of pins are multifunctioned.	More number pins are multifunctioned.

8051 MICROCONTROLLER HARDWARE

- It is a 40 pin dual in line (DIP) package.
- It have unique features like
- ❖ internal ROM and RAM.
- ❖ i/o ports with programmable pins.
- ❖ timers and counters.
- ❖ serial data communication.

The 8051 architecture consists of these specific features :

- 8-bit CPU with registers A (accumulator) and B.
- 16-bit program counter (pc) and data pointer (DPTR).
- 8-bit program status word (PSW).
- 8-bit stack pointer (SP).
- Internal ROM or EPROM of 0 to 4k.
- Internal ram of 128 bytes:
- ✓ 4 register banks, each consisting of 8 registers.
- ✓ 16 bytes ,which may be addressed at a bit level.
- ✓ 80 bytes of general purpose data memory.
- 32 I/O pins arranged as four 8-bit ports: P0-P3.
- Two 16-bit timer/counters : t0 and t1.
- Full duplex serial data receiver/transmitter: SBUF.
- Control registers :TCON, TMOD, SCON, PCON, IP, IE.
- 2 external and 3 internal interrupt sources.
- Oscillator and clock circuits.